## CLAIMS

What is claimed is:

1. A method for refreshing data in a dynamic circuit element having an input terminal and an output terminal, the method comprising the operations of:

(a) coupling a static loop to the dynamic circuit element as a feedback path from the output terminal to the input terminal;

(b) providing a control signal to the static loop; and

(c) activate the static loop via the control signal to refresh the data in the dynamic circuit element.

2. The method of claim 1 further comprising the operation of:

setting the control signal equal to approximately zero to deactivate the static loop so that the dynamic circuit element operates in a dynamic mode.

3. The method of claim 1 wherein the dynamic circuit element is a inverter included in a dynamic register.

4. The method of claim 3 wherein operation (a) comprises:

coupling a first transistor to the output terminal of the dynamic circuit element;

coupling a second transistor to the input terminal of the dynamic circuit element;

coupling an input of a loop inverter to the first transistor and an output of the loop inverter to the second transistor; and

coupling gate terminals of the first and second transistors to the control signal.

5. The method of claim 4 further comprising the operations of:

(1) coupling the gate terminal of the first transistor and the input of the loop inverter to an auxiliary circuit, the auxiliary circuit including an auxiliary transistor and receiving the control signal;

(2) turning on the auxiliary transistor via the control signal to apply a fixed voltage to the input of the loop inverter when the first transistor is off; and

(3) turning off the auxiliary transistor via the control signal so that the auxiliary circuit does not affect the voltage at the input of the loop inverter when the first transistor is on.

6. The method of claim 5 wherein operation (1) comprises the operations of:

coupling the gate terminal of the first transistor to an input of an auxiliary inverter;

coupling an output of the auxiliary inverter to a gate terminal of an N-type MOS transistor, the N-type MOS transistor being the auxiliary transistor; and

coupling a drain terminal of the N-type MOS transistor to the input of the loop inverter; and

coupling a source terminal of the N-type MOS transistor to ground.

7. The method of claim 5 wherein operation (1) comprises the operation of:

coupling the gate terminal of the first transistor to a gate terminal of a P-type MOS transistor, the P-type MOS transistor being the auxiliary transistor; and

coupling a drain terminal of the P-type MOS transistor to the input of the loop inverter; and

coupling a source terminal of the P-type MOS transistor to a positive voltage source.

8. A method for refreshing a dynamic register, the dynamic register comprising a first transmission gate and a second transmission gate operating in accordance with complementary clock signals, a first inverter disposed between the first and second transmission gates, a second inverter disposed at the output of the second transmission gate, the first inverter having a first input terminal and a first output terminal, the second inverter having a second input terminal and a second output terminal, the method comprising the operations of:

(a) coupling a first static loop to the first inverter as a feedback path from the first output terminal to the first input terminal;

(b) coupling a second static loop to the second inverter as a feedback path from the second output terminal to the second input terminal;

(c) providing a control signal to the first and second static loops; and

(d) activate the first and second static loops via the control signal to refresh the dynamic register.

9. The method of claim 8 further comprising the operation of:

setting the control signal equal to approximately zero to deactivate the first and second static loops so that the dynamic register operates in a dynamic mode.

10. The method of claim 8 wherein operation (a) comprises:

coupling a first transistor to the first output terminal of the first inverter;

coupling a second transistor to the first input terminal of the first inverter;

coupling an input of a first loop inverter to the first transistor and an output of the first loop inverter to the second transistor;

coupling gate terminals of the first and second transistors to the control signal;

coupling a third transistor to the second output terminal of the second inverter;

coupling a fourth transistor to the second input terminal of the second inverter;

coupling an input of a second loop inverter to the third transistor and an output of the second loop inverter to the fourth transistor; and

coupling gate terminals of the third and fourth transistors to the control signal.

11. The method of claim 10 further comprising the operations of:

(1) coupling the gate terminal of the first transistor and the input of the first loop inverter to a first auxiliary circuit, the first auxiliary circuit including a first auxiliary transistor and receiving the control signal;

(2) turning on the first auxiliary transistor via the control signal to apply a fixed voltage to the input of the first loop inverter when the first transistor is off;

(3) turning off the first auxiliary transistor via the control signal so that the first auxiliary circuit does not affect a voltage at the input of the first loop inverter when the first transistor is on;

(4) coupling the gate terminal of the third transistor and the input of the second loop inverter to a second auxiliary circuit, the second auxiliary circuit including a second auxiliary transistor and receiving the control signal;

(5) turning on the second auxiliary transistor via the control signal to apply the fixed voltage to the input of the second loop inverter when the third transistor is off; and

(6) turning off the second auxiliary transistor via the control signal so that the second auxiliary circuit does not affect a voltage at the input of the second loop inverter when the third transistor is on.

12. The method of claim 11 wherein operation (1) comprises the operations of:

coupling the gate terminal of the first transistor to an input of a first auxiliary inverter;

coupling an output of the first auxiliary inverter to a gate terminal of a first N-type MOS transistor, the first N-type MOS transistor being the first auxiliary transistor;

coupling a drain terminal of the first N-type MOS transistor to the input of the first loop inverter; and

coupling a source terminal of the first N-type MOS transistor to ground;

and wherein operation (4) comprises the operations of:

coupling the gate terminal of the third transistor to an input of a second auxiliary inverter;

coupling an output of the second auxiliary inverter to a gate terminal of a second N-type MOS transistor, the second N-type MOS transistor being the second auxiliary transistor;

coupling a drain terminal of the second N-type MOS transistor to the input of the second loop inverter; and

coupling a source terminal of the second N-type MOS transistor to ground.

13. The method of claim 11 wherein operation (1) comprises the operation of:

coupling the gate terminal of the first transistor to a gate terminal of a first P-type MOS transistor, the first P-type MOS transistor being the first auxiliary transistor;

coupling a drain terminal of the first P-type MOS transistor to the input of the first loop inverter;

coupling a source terminal of the first P-type MOS transistor to a positive voltage source;

and wherein operation (4) comprises the operations of:

coupling the gate terminal of the third transistor to a gate terminal of a second P-type MOS transistor, the second P-type MOS transistor being the second auxiliary transistor;

coupling a drain terminal of the second P-type MOS transistor to the input of the second loop inverter; and

coupling a source terminal of the second P-type MOS transistor to a positive voltage source.

14. A system for refreshing a dynamic register, the dynamic register comprising a first transmission gate and a second transmission gate operating in accordance with complementary clock signals, a first inverter disposed between the first and second transmission gates, a second inverter disposed at the output of the second transmission gate, the first inverter having a first input terminal and a first output terminal, the second inverter having a second input terminal and a second output terminal, the system comprising:

(a) a first static loop coupled to the first inverter as a feedback path from the first output terminal to the first input terminal, the first static loop receiving a control signal, the first static loop being activated or deactivated by the control signal, the first static loop refreshing the first inverter when activated; and

(b) a second static loop coupled to the second inverter as a feedback path from the second output terminal to the second input terminal, the second static loop receiving a control signal, the second static loop being activated or deactivated by the control signal, the second static loop refreshing the second inverter when activated.

15. The system of claim 14 wherein the first and second static loops are deactivated when the control signal is approximately equal to zero.

16. The system of claim 14 wherein the first static loop comprises:

a first transistor coupled to the first output terminal of the first inverter, a gate terminal of the first transistor being coupled to the control signal;

a second transistor coupled to the first input terminal of the first inverter, a gate terminal of the second transistor being coupled to the control signal; and

a first loop inverter having an input coupled to the first transistor and an output coupled to the second transistor;

and wherein the second static loop comprises:

a third transistor coupled to the second output terminal of the second inverter, a gate terminal of the third transistor being coupled to the control signal;

a fourth transistor coupled to the second input terminal of the second inverter, a gate terminal of the fourth transistor being coupled to the control signal; and

a second loop inverter having an input coupled to the third transistor and an output coupled to the fourth transistor.

17. The system of claim 16 further comprising:

(1) a first auxiliary circuit coupled to the gate terminal of the first transistor and to the input of the first loop inverter, the first auxiliary circuit including a first auxiliary transistor and receiving the control signal, the first auxiliary transistor being turned on via the control signal to apply a fixed voltage to the input of the first loop inverter when the first transistor is off, the first auxiliary transistor being turned off via the control signal so that the first auxiliary circuit does not affect a voltage at the input of the first loop inverter when the first transistor is on; and

(2) a second auxiliary circuit coupled to the gate terminal of the third transistor and to the input of the second loop inverter, the second auxiliary circuit including a second auxiliary transistor and receiving the control signal, the second auxiliary transistor being turned on via the control signal to apply a fixed voltage to the input of the second loop inverter when the third transistor is off, the second auxiliary transistor being turned off via the control signal so that the second auxiliary circuit does not affect a voltage at the input of the second loop inverter when the third transistor is on.

18. The system of claim 17 wherein the first auxiliary circuit comprises:

a first auxiliary inverter having an input coupled to the gate terminal of the first transistor; and

a first N-type MOS transistor having a gate terminal coupled to an output of the first auxiliary inverter, a drain terminal coupled to the input of the first loop inverter and a source terminal coupled to ground, the first N-type MOS transistor being the first auxiliary transistor;

and wherein the second auxiliary circuit comprises:

a second auxiliary inverter having an input coupled to the gate terminal of the third transistor ; and

a second N-type MOS transistor having a gate terminal coupled to an output of the second auxiliary inverter, a drain terminal coupled to the input of the second loop inverter and a source terminal coupled to ground, the second N-type MOS transistor being the second auxiliary transistor.

19. The system of claim 17 wherein the first auxiliary circuit comprises:

a first P-type MOS transistor having a gate terminal coupled to the gate terminal of the first transistor, a drain terminal coupled to the input of the first loop inverter and a source terminal coupled to a positive voltage source, the first P-type MOS transistor being the first auxiliary transistor;

and wherein the second auxiliary circuit comprises:

a second P-type MOS transistor having a gate terminal coupled to the gate terminal of the third transistor, a drain terminal coupled to the input of the second loop inverter and a source terminal coupled to a positive voltage source, the second P-type MOS transistor being the second auxiliary transistor.

20. The system of claim 14 wherein the dynamic register is included in a gigabit transceiver chip.